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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/996,091	11/28/2001	Hayden Clavie Cranford JR.	RAL920010004US2 (IRA-10-5	2524

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EXAMINER	
CLEARY, THOMAS J	
ART UNIT	**PAPER NUMBER**
2111	

DATE MAILED: 12/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/996,091	CRANFORD ET AL.	
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 1, 5, 6, 9, 10, 11, 15, 16, 19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent number 5,115,450 to Arcuri ("Arcuri") and US Patent Number 5,943,378 to Keba et al. ("Keba").

3. In reference to Claim 1, Arcuri teaches a method of transferring stored digital parallel data of multiple bits of data stored in a first data register (See Figure 4 Number 54) from a transmitter (See Figure 3 Number 20) to a receiver (See Figure 3 Number 21) over a hard wired conductor (See Figure 3 Number 23) comprising the steps of: synchronously converting said stored digital data to a serial analog data signal in said transmitter (See Figure 4 Number 57); transmitting said serial signal asynchronously over said hard wired conductor to said receiver (See Column 3 Lines 48-52); and restoring said asynchronous serial analog signal to synchronous digital parallel data in said receiver corresponding to the data stored in said first data register in said

transmitter (See Figure 5 Number 83). Arcuri further teaches that the digital data is synchronized with a clock signal (See Column 3 Lines 19-21). Arcuri further teaches that the analog to digital converter asynchronously converts the analog levels in the analog output to multi-bit digital outputs (See Column 2 Lines 10-12), and thus the analog signal is an asynchronous signal. Arcuri does not teach detecting both edges of the data in said asynchronous serial signal for conversion to parallel data bits and using a phase rotator to convert said asynchronous signal to said synchronous digital parallel data in conjunction with said edge detection. Arcuri teaches an analog to digital converter (See Figure 5 Number 83), but is silent as to the construction of it. Keba teaches a system that performs serial analog to parallel digital conversion (See Column 2 Lines 57-62) on a received signal using a symbol recovery unit (See Figures 1 and 3 Number 112) which comprises and edge detection unit (See Figure 2 Number 205) for detecting both edges of the data by generating a pulse whenever the signal exhibits an edge (See Column 3 Lines 48-51). Keba further teaches a PLL which uses the edge signal to adjust the phase of a clock signal based on the pulses of the edge signal, and thus performing an equivalent function to a phase rotator, for converting the asynchronous signal to a synchronous signal (See Figure 2 Number 225 and Column 3 Lines 51-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Arcuri using the symbol recovery unit of Keba to perform analog to digital conversion, resulting in the invention of Claim 1, because it is a conventional manner for optimizing the clock to have its positive edges

near the center of each symbol period (See Column 3 Lines 53-57 of Keba), because it allows information to be recovered from the signal with minimal errors (See Column 1 Lines 18-21 of Keba), and because it can be used as an alternative to an analog to digital converter (See Column11 Lines 4-7 of Keba).

4. Claim 11 recites limitations which are substantially equivalent to those of Claim 1, and thus is rejected under similar reasoning as applied to Claim 1 above.

5. In reference to Claim 5, Arcuri and Keba teach the limitations as applied to Claim 1 above. Arcuri further teaches that the data in the first register is comprised of eight bits (See Figure 8 Number 200).

6. Claim 15 recites limitations which are substantially equivalent to those of Claim 5, and thus is rejected under similar reasoning as applied to Claim 15 above.

7. In reference to Claim 6, Arcuri and Keba teach the limitations as applied to Claim 1 above. Arcuri further teaches that a clocking signal is used to convert the analog serial signal to a digital signal (See Figure 5 Number 80).

8. Claim 16 recites limitations which are substantially equivalent to those of Claim 6, and thus is rejected under similar reasoning as applied to Claim 16 above.

9. In reference to Claim 9, Arcuri and Keba teach the limitations as applied to Claim 1 above. Keba further teaches that edges are derived from multiple samples (See Column 4 Lines 4-13).

10. Claim 19 recites limitations which are substantially equivalent to those of Claim 9, and thus is rejected under similar reasoning as applied to Claim 9 above.

11. In reference to Claim 10, Arcuri and Keba teach the limitations as applied to Claim 9 above. Keba further teaches that the multiple samples are used to determine the approximate center of the resulting data bit (See Column 3 Lines 53-57).

12. Claim 20 recites limitations which are substantially equivalent to those of Claim 10, and thus is rejected under similar reasoning as applied to Claim 10 above.

13. Claims 2, 3, 4, 12, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arcuri and Keba as applied to Claim 1 above, and further in view of US Patent Number 6,222,380 to Gerowitz et al. ("Gerowitz").

14. In reference to Claim 2, Arcuri and Keba teach the limitations as applied to Claim 1 above. Arcuri and Keba do not teach that the digital parallel data is read out of the first data register into at least one single bit latch. Arcuri teaches parallel to serial

conversion but is silent as to how it is performed. Gerowitz teaches a parallel to serial converter that reads data into at least one single bit latch (See Figure 2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Arcuri and Keba using the parallel to serial conversion device of Gerowitz, resulting in the invention of Claim 2, in order to allow the data to be transmitted over a high-speed, high-volume data path that uses fewer pins and transfers data at a faster rate than a traditional bus structure (See Column 2 Lines 16-20 of Gerowitz).

15. Claim 12 recites limitations which are substantially equivalent to those of Claim 2, and thus is rejected under similar reasoning as applied to Claim 2 above.

16. In reference to Claim 3, Arcuri, Keba, and Gerowitz teach the limitations as applied to Claim 2 above. Gerowitz further teaches that the data is read N bits at a time (See Figure 2 D0-D3), each data bit to a different one of the N latches (See Figure 2 LATCH L1 – LATCH L4), and from each latch to another latch (See Figure 2 LATCH L5), and clocking an additional N bits of data to be subsequently written to said N latch and to said another latch until all bits of data have been read (See Column 4 Line 64 – Column 5 Line 4). Arcuri, Keba, and Gerowitz do not expressly teach that the data is read out from said first register in said transmitter two bits at a time, each data bit to first and second single data bit latch, and from each first and second single bit data latch to a third single bit data latch, clocking additional two data bits to be subsequently written

to said first and second one bit latch and to said third single bit data latch until all bits of the data have been read from the first latch. Gerowitz shows an exemplary embodiment where N is equal to 4; however, N can represent any integer, including 2. The portion of the specification describing the use of two single bit registers states that "It is to be understood that other than two bits at a time can be read from the register 24. However this number must be a number that is evenly divisible into the number of bits in the register 24."

It would have been obvious to one of ordinary skill in the art at the time the invention was made to read the data out from said first register in said transmitter two bits at a time, each data bit to first and second single data bit latches, and from each first and second single bit data latch to a third single bit data latch, clocking an additional two data bits to be subsequently written to said first and second one bit latches and to said third single bit data latch until all bits of the data have been read from the first register, resulting in the invention of Claim 3, because Applicant has not disclosed that the use of two latches provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with either the four latches in the exemplary embodiment taught by Gerowitz or the two latches taught by Applicant because both perform the same function of converting a parallel data signal to a serial data signal, and because the N latches taught by Gerowitz can represent any integer number of latches. Therefore, it would have been obvious to one of ordinary skill in the art to modify Arcuri, Keba, and Gerowitz to obtain the invention as specified in Claim 3.

17. Claim 13 recites limitations which are substantially equivalent to those of Claim 3, and thus is rejected under similar reasoning as applied to Claim 3 above.

18. In reference to Claim 4, Arcuri, Keba, and Gerowitz teach the limitations as applied to Claim 3 above. Gerowitz further teaches that the bits from the third single bit latch are converted to a single serial analog signal of the data (See Figure 2 Signal Q and Column 5 Lines 5-15).

19. Claim 14 recites limitations which are substantially equivalent to those of Claim 4, and thus is rejected under similar reasoning as applied to Claim 14 above.

20. Claims 7, 8, 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arcuri, Keba, and Gerowitz as applied to Claim 3 above, and further in view of US Patent Number 5,202,979 to Hillis et al. ("Hillis").

21. In reference to Claim 7, Arcuri, Keba, and Gerowitz teach the limitations as applied to Claim 3 above. Arcuri, Keba, and Gerowitz do not teach said analog signal is converted in said receiver to two one-bit signals and delivered to a shift latch and then stored in a second data latch. Arcuri further teaches storing the converted bits in a second data register (See Figure 5 Number 85). Arcuri teaches serial to parallel conversion (See Figure 5) but is silent as to the details of how it is accomplished. Hillis

teaches a shift register that takes two bits from a serial input signal and shifts them two bits at every clock pulse before shifting the accumulated bits out in parallel (See Figure 3 Number 34 and Column 3 Line 49 – Column 4 Line 15).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Arcuri, Keba, and Gerowitz with the 2 bit shift register of Hillis, resulting in the invention of Claim 7, in order to speed up data transfer by only needing half as many clock pulses to accumulate the data from the input line (See Column 4 Lines 8-10 of Hillis), as well as to reduce power consumption since fewer clock transitions are required.

22. Claim 17 recites limitations which are substantially equivalent to those of Claim 7, and thus is rejected under similar reasoning as applied to Claim 7 above.

23. In reference to Claim 8, Arcuri, Keba, Gerowitz, and Hillis teach the limitations as applied to Claim 7 above. Arcuri further teaches that data bits are delivered synchronously to the second data register (See Figure 5 Numbers 77, 79, 80, and 81).

24. Claim 18 recites limitations which are substantially equivalent to those of Claim 8, and thus is rejected under similar reasoning as applied to Claim 8 above.

Claim Rejections - 35 USC § 112

25. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

26. Claims 7, 8, 17, and 18 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 7 and 17 recite the limitations of using latches. However, both the specification (See Page 7 Paragraph 1) and the drawings (See Figure 3 Numbers 64 and 68) disclose using registers. It is unclear if the Applicant intends for registers and latches to be interpreted as functionally equivalent devices. For the purpose of evaluating prior art, the Examiner will assume that registers and latches perform an equivalent function.

27. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the Applicant regards as his invention.

28. Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant

regards as the invention. Claim 4 recites the limitation "the third single bit register" in Line 2. There is insufficient antecedent basis for this limitation in the claim.

Response to Arguments

29. Applicant's arguments filed 11 October 2005 have been fully considered but they are not persuasive.

30. Applicant has argued that Arcuri does not teach conversion of a synchronous digital signal to an asynchronous analog signal for transmission, and reconverting the asynchronous analog signal upon receipt to a synchronous digital signal. In response, the Examiner notes that Arcuri teaches that the digital data is synchronized with a clock signal (See Column 3 Lines 19-21). Arcuri further teaches that the analog to digital converter asynchronously converts the analog levels in the analog output to multi-bit digital outputs (See Column 2 Lines 10-12), and thus the analog signal is an asynchronous signal. Thus, Arcuri teaches conversion of a synchronous digital signal to an asynchronous analog signal for transmission, and reconverting the asynchronous analog signal upon receipt to a synchronous digital signal.

31. Applicant has argued that Keba does not teach detection of both edges. In response, the Examiner notes that Keba teaches multiple embodiments of an analog to digital converter, both of which have components for detecting both edges of a signal.

The first embodiment samples a signal multiple times and produces a pulse when an edge is detected in the signal (See Column 3 Lines 48-51). The second embodiment takes multiple samples of a signal and produces an "edge signal" at every zero crossing transition time, which occurs whenever the sign of the signal changes state, which occurs at the edges of the signal. Thus, Keba teaches the detection of both edges of a signal.

32. Applicant has argued that the PLL of Keba is not a phase rotator. In response, the Examiner notes that the PLL of Keba "uses the edge signal 206 to adjust the phase of the symbol clock signal 226 based on the pulses of the edge signal 206". As a phase rotator is used for producing a controlled phase shift, the system of Keba is functioning in a manner which is logically equivalent to a phase rotator.

33. Applicant has argued that Keba does not teach multiple signals used to derive each edge. In response, the Examiner notes that the features upon which Applicant relies (i.e., multiple signals used to derive each edge) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Claims 9, 10, 19, and 20 require multiple samples to derive each edge. Further, the first embodiment of Keba teaches detecting when the value of a signal changes, thus denoting an edge. In order to determine when the value of the signal changes, multiple samples of the signal must be taken and compared.

Likewise, in the second embodiment, an oversampled level decoder is used to produce a signal indicating the sign of the value of the signal, which indicates a zero crossing transition time, and thus, an edge.

34. Applicant has argued that there is no motivation for modifying Arcuri and Keba with Gerowitz. In response, the Examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, it would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Arcuri and Keba using the parallel to serial conversion device of Gerowitz in order to allow the data to be transmitted over a high-speed, high-volume data path that uses fewer pins and transfers data at a faster rate than a traditional bus structure (See Column 2 Lines 16-20 of Gerowitz)..

35. Applicant has argued that Hillis does not teach converting the analog signal in the receiver into two one-bit signals, delivering them to a shift latch, and storing them in a second latch. In response, the Examiner notes that Arcuri teaches storing the converted bits in a second data register (See Figure 5 Number 85). Arcuri further teaches serial to parallel conversion (See Figure 5) but is silent as to the details of how

it is accomplished. Hillis teaches a shift register that takes two bits from a serial input signal and shifts them two bits at every clock pulse before shifting the accumulated bits out in parallel (See Figure 3 Number 34 and Column 3 Line 49 – Column 4 Line 15). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Arcuri, Keba, and Gerowitz with the 2 bit shift register of Hillis in order to speed up data transfer by only needing half as many clock pulses to accumulate the data from the input line (See Column 4 Lines 8-10 of Hillis), as well as to reduce power consumption since fewer clock transitions are required.

Conclusion

36. The following prior art made of record and not relied upon is considered pertinent to Applicant's disclosure: US Patent Application Publication Number 2004/0218705 to Cranford et al.

37. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Thomas J. Cleary whose telephone number is 571-272-3624. The Examiner can normally be reached on Monday-Thursday (7-3), Alt. Fridays (7-2).

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TJC

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12/16/05